

## ABSTRACT

1 An application specific integrated circuit (ASIC) is disclosed. The ASIC includes a  
2 standard cell. The standard cell includes a plurality of logic functions and at least one bus  
3 coupled to at least a portion of the logic functions. The standard cell also includes a plurality  
4 of internal signals from the plurality of logic functions and a field programmable gate array  
5 (FPGA) function coupled to the at least one bus and at least a portion of the plurality of internal  
6 signals. The FPGA function includes a debug client function that observes and manipulates  
7 the at least one bus and the plurality of internal signals. A system and method in accordance  
8 with the present invention utilizes a debug function within a standard cell design to create an  
9 internal-to-the-ASIC debugging (software, hardware or both) function. The system and  
10 method is provided by connection of internal buses and signals of interest to a debug client  
11 function within the FPGA function. The debug client function observes and, if needed,  
12 manipulates internal buses and signals and communicates with an external to the ASIC  
13 debugging system.